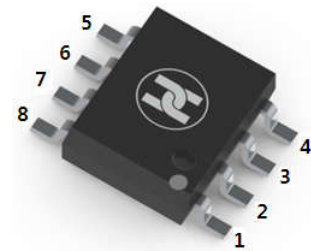


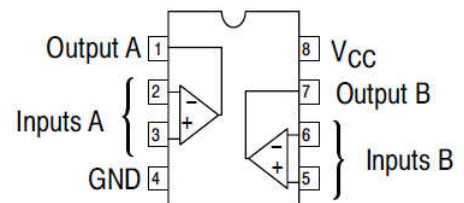
LOW OFFSET VOLTAGE DUAL COMPARATORS

FEATURES

- Wide single-supply range: 2.0Vdc to 36Vdc
- Split-supply range: ± 1.0 Vdc to ± 18 Vdc
- Very low current drain independent of supply voltage: 0.4mA
- Low input bias current: 25nA
- Low input offset current: 5.0nA
- Low input offset voltage: 5.0mV (max)
- Input common mode range to ground level
- Differential input voltage range equal to power supply voltage
- Output voltage compatible with DTL,ECL,TTL, MOS,and CMOS Logic levels
- ESD clamps on the inputs increase the ruggedness of the device without affecting performance



SOP-8



MECHANICAL DATA

- Case: SOP-8
- Case material: Molded plastic. UL flammability
- Classification rating: 94V-0
- Terminal: Tin plated,solderable per MIL-STD-750, method 2026
- Weight: 0.3grams (approximate)

MAXIMUM RATINGS($T_A=25^{\circ}\text{C}$ unless otherwise specified)

Parameter		Symbol	Value	Unit
Power supply voltage		V_{CC}	+36 or ± 18	Vdc
Input differential voltage range		V_{IDR}	36	Vdc
Input common mode voltage range		V_{ICR}	$-0.3 \sim +36$	Vdc
Output short circuit-to-ground		I_{SC}	Continuous	mA
Output sink current (note 1)		I_{Sink}	20	
Power dissipation	$T_A = 25^{\circ}\text{C}$	P_D	570	mW
	Derate above 25°C	$1/R_{\theta JA}$	5.7	mW/ $^{\circ}\text{C}$
Operating ambient temperature range		T_A	$0 \sim +70$	$^{\circ}\text{C}$
Maximum operating junction temperature		$T_{J(max)}$	150	$^{\circ}\text{C}$
Storage temperature range		T_{stg}	$-65 \sim +150$	$^{\circ}\text{C}$
ESD protection at any pin	Human body model	V_{ESD}	1500	V
	Machine model		150	

Note:

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied,damage may occur and reliability may be affected.

1. The maximum output current may be as high as 20mA, independent of the magnitude of V_{CC} , output short circuits to V_{CC} can cause excessive heating and eventual destruction.

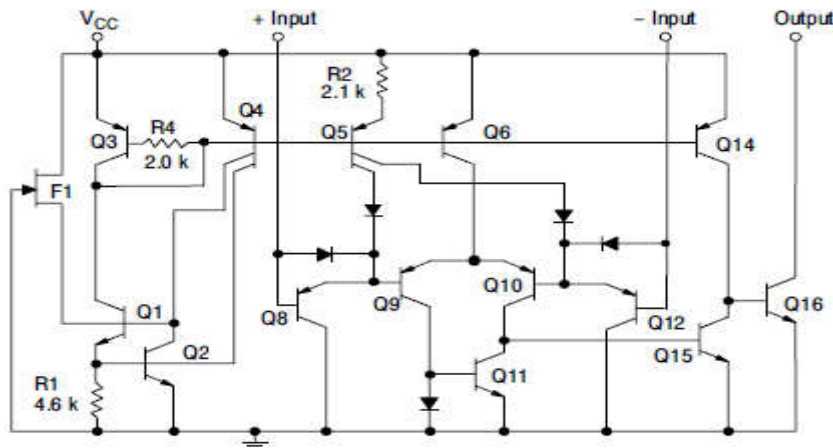
LOW OFFSET VOLTAGE DUAL COMPARATORS

ELECTRICAL CHARACTERISTICS ($V_{CC}=5.0V_{dc}$, $0^{\circ}C \leq T_A \leq +70^{\circ}C$, unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input offset voltage (note 3)	V_{IO}		± 1.0	± 5.0	mV	$T_A = 25^{\circ}C$
				9.0		$0^{\circ}C \leq T_A \leq +70^{\circ}C$
Input offset current	I_{IO}		± 5.0	± 50	nA	$T_A = 25^{\circ}C$
				± 150		$0^{\circ}C \leq T_A \leq +70^{\circ}C$
Input bias current (note 4)	I_{IB}		25	250	nA	$T_A = 25^{\circ}C$
				400		$0^{\circ}C \leq T_A \leq +70^{\circ}C$
Input common mode voltage range (note 4)	V_{ICR}	0		$V_{CC} - 1.5$	V	$T_A = 25^{\circ}C$
		0		$V_{CC} - 2.0$		$0^{\circ}C \leq T_A \leq +70^{\circ}C$
Voltage gain	A_{VOL}	50	200		V/mV	$R_L \geq 15k, V_{CC} = 15V_{dc}, T_A = 25^{\circ}C$
Large signal response time			300		ns	$V_{in} = \text{TTL logic swing}, V_{ref} = 1.4V_{dc}$ $V_{RL} = 5.0V_{dc}, R_L = 5.1k, T_A = 25^{\circ}C$
Response time (note 6)	t_{TLH}		1.3		μs	$V_{RL} = 5.0V_{dc}, R_L = 5.1k, T_A = 25^{\circ}C$
Input differential voltage (note 7)	V_{ID}			V_{CC}	V	All $V_{in} \geq GND$ or V -Supply (if used)
Output sink current	I_{Sink}	6.0	16		mA	$V_{in} \geq 1.0V_{dc}, V_{in+} = 0V_{dc},$ $V_o \leq 1.5V_{dc}, T_A = 25^{\circ}C$
Output saturation voltage	V_{OL}		150	400	mV	$V_{in} \geq 1.0V_{dc}, V_{in+} = 0, I_{Sink} \leq 4.0mA,$ $T_A = 25^{\circ}C$
				700		$0^{\circ}C \leq T_A \leq +70^{\circ}C$
Output leakage current	I_{OL}		0.1		nA	$V_{in-} = 0V, V_{in+} \geq 1.0V_{dc},$ $V_o = 5.0V_{dc}, T_A = 25^{\circ}C$
				1000		$V_{in-} = 0V, V_{in+} \geq 1.0V_{dc},$ $V_o = 30V_{dc}, 0^{\circ}C \leq T_A \leq +70^{\circ}C$
Supply current	I_{CC}		0.4	1.0	mA	$R_L = \infty$ both comparators, $T_A = 25^{\circ}C$
				2.5		$R_L = \infty$ both comparators, $V_{CC} = 30V$

- Note: 2. The maximum output current may be as high as 20mA, independent of the magnitude of V_{CC} , output short circuits to V_{CC} can cause excessive heating and eventual destruction.
3. At output switch point, $V_o \approx 1.4V_{dc}$, $R_s = 0\Omega$ with V_{CC} from $5.0V_{dc}$ to $30V_{dc}$, and over the full input common mode range ($0V$ to $V_{CC} - 1.5V$).
4. Due to the PNP transistor inputs, bias current will flow out of the inputs. This current is essentially constant, independent of the output state, therefore, no loading changes will exist on the input lines.
5. Input common mode of either input should not be permitted to go more than $0.3V$ negative of ground or minus supply. The upper limit of common mode range is $V_{CC} - 1.5V$.
6. Response time is specified with a $100mV$ step and $5.0mV$ of overdrive. With larger magnitudes of overdrive faster response times are obtainable.
7. The comparator will exhibit proper output state if one of the inputs becomes greater than V_{CC} , the other input must remain within the common mode range. The low input state must not be less than $-0.3V$ of ground or minus supply.

REPRESENTATIVE SCHEMATIC DIAGRAM (DIAGRAM SHOWN IS FOR 1 COMPARATOR)



LOW OFFSET VOLTAGE DUAL COMPARATORS

TYPICAL CHARACTERISTICS

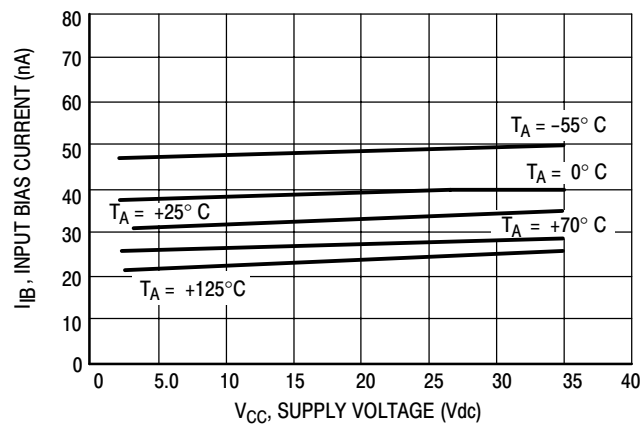


Figure 1. Input Bias Current versus Power Supply Voltage

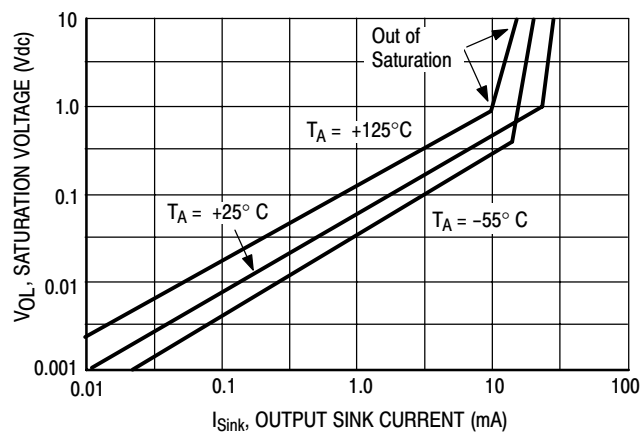


Figure 2. Output Saturation Voltage versus Output Sink Current

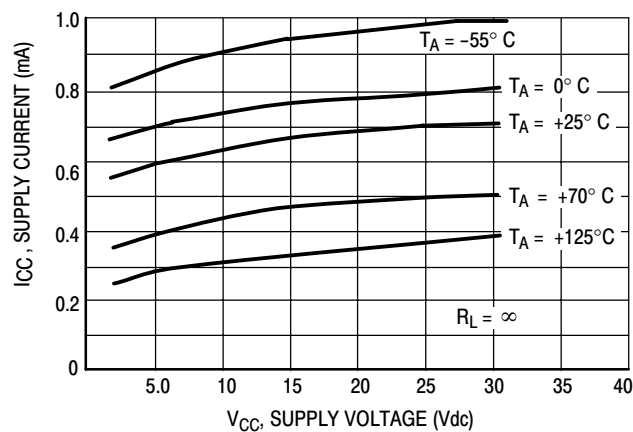
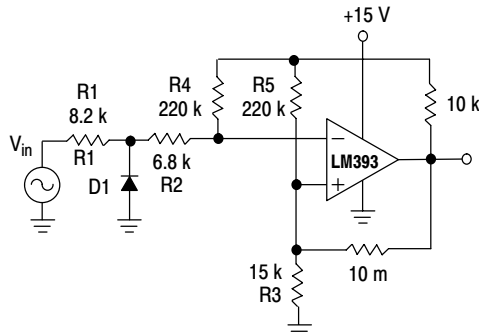


Figure 3. Power Supply Current versus Power Supply Voltage

LOW OFFSET VOLTAGE DUAL COMPARATORS

APPLICATIONS INFORMATION

These dual comparators feature high gain, wide bandwidth characteristics. This gives the device oscillation tendencies if the outputs are capacitively coupled to the inputs via stray capacitance. This oscillation manifests itself during output transitions (V_{OL} to V_{OH}). To alleviate this situation, input resistors $< 10\text{ k}\Omega$ should be used.



D1 prevents input from going negative by more than 0.6 V.

$$R1 + R2 = R3$$

$$R3 \leq \frac{R5}{10} \text{ for small error in zero crossing.}$$

Figure 4. Zero Crossing Detector (Single Supply)

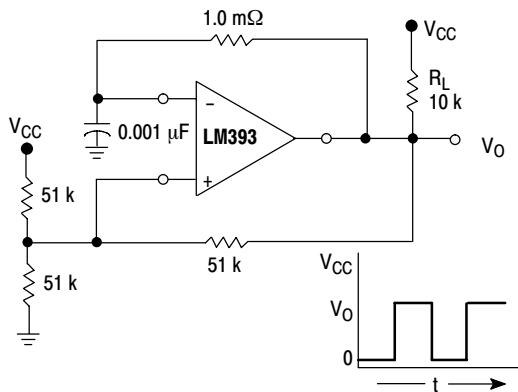
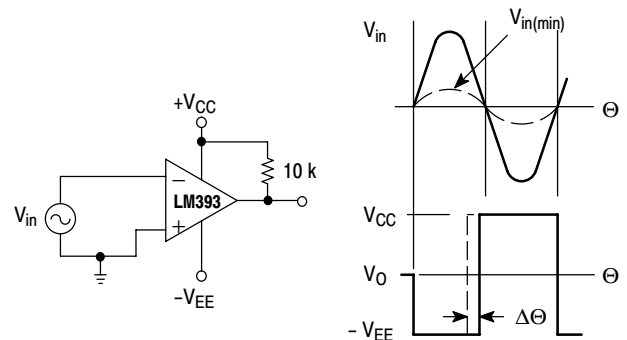


Figure 6. Free-Running Square-Wave Oscillator

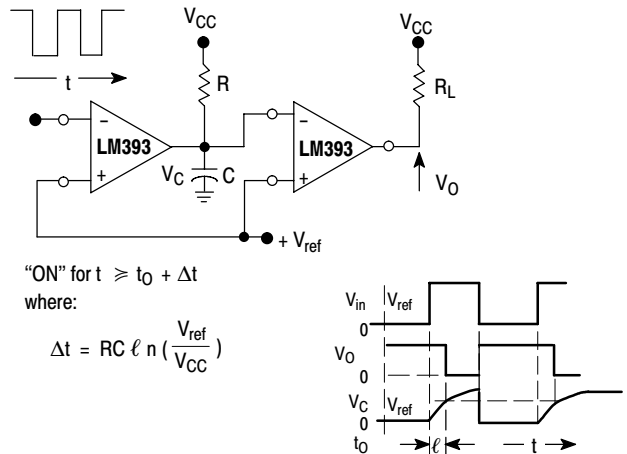
The addition of positive feedback ($< 10\text{ mV}$) is also recommended. It is good design practice to ground all unused pins.

Differential input voltages may be larger than supply voltage without damaging the comparator's inputs. Voltages more negative than -0.3 V should not be used.



$$V_{in(min)} \approx 0.4\text{ V peak for } 1\% \text{ phase distortion } (\Delta\theta).$$

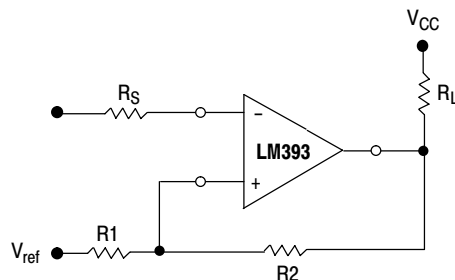
Figure 5. Zero Crossing Detector (Split Supply)



"ON" for $t \geq t_0 + \Delta t$
where:

$$\Delta t = RC \ln \left(\frac{V_{ref}}{V_{CC}} \right)$$

Figure 7. Time Delay Generator



$$R_S = R1 \parallel R2$$

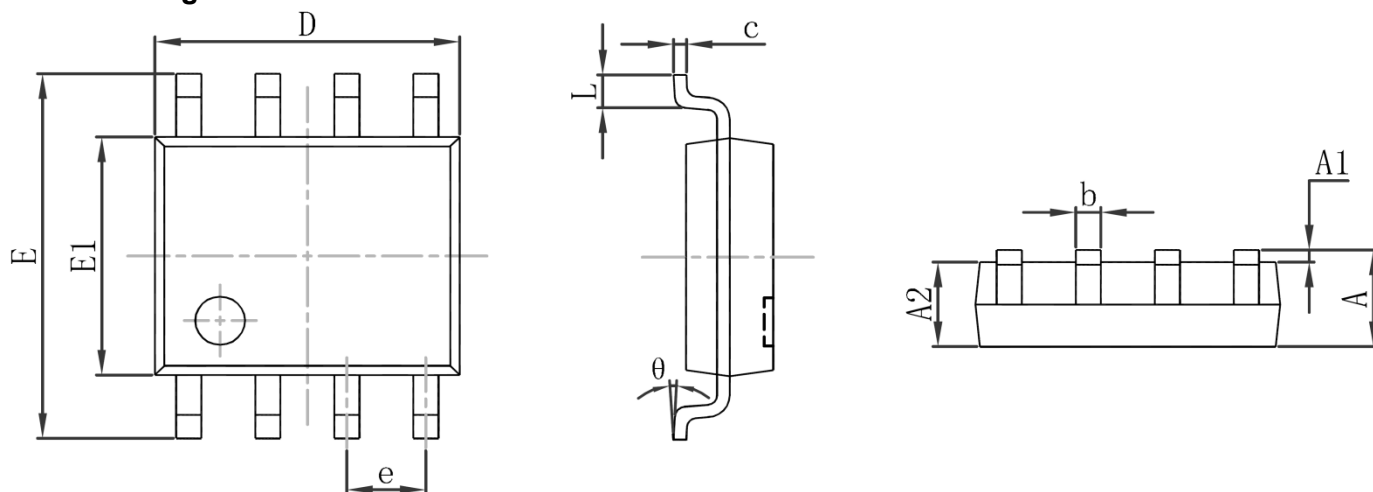
$$V_{th1} = V_{ref} + \frac{(V_{CC} - V_{ref}) R1}{R1 + R2 + R_L}$$

$$V_{th2} = V_{ref} - \frac{(V_{ref} - V_{OL}) R1}{R1 + R2}$$

Figure 8. Comparator with Hysteresis

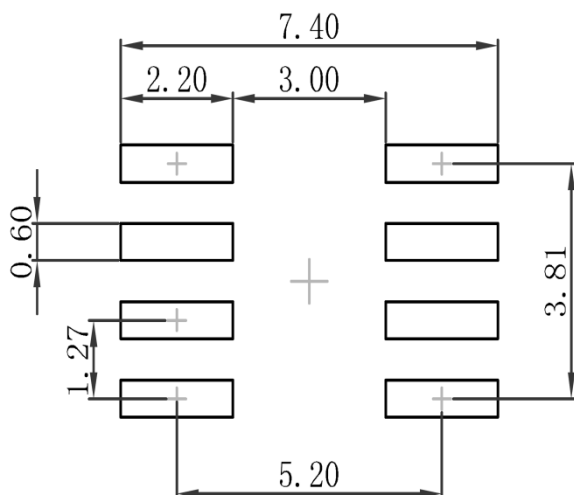
LOW OFFSET VOLTAGE DUAL COMPARATORS

SOP-8 Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270(BSC)		0.050 (BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

SOP-8 Suggested Pad Layout



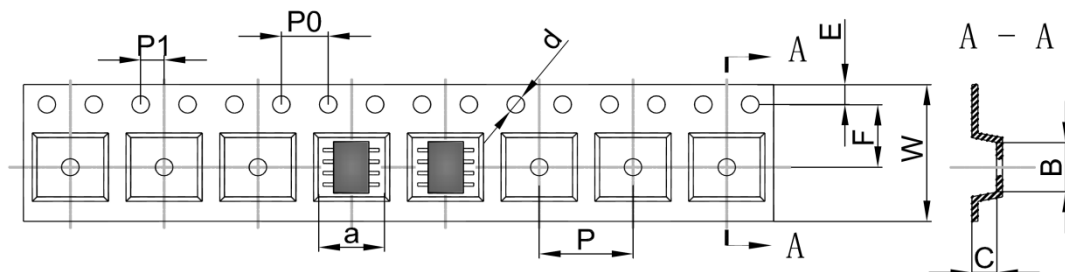
Note:

1. Controlling dimension: in millimeters
2. General tolerance: $\pm 0.05\text{mm}$
3. The pad layout is for reference purposes only

LOW OFFSET VOLTAGE DUAL COMPARATORS

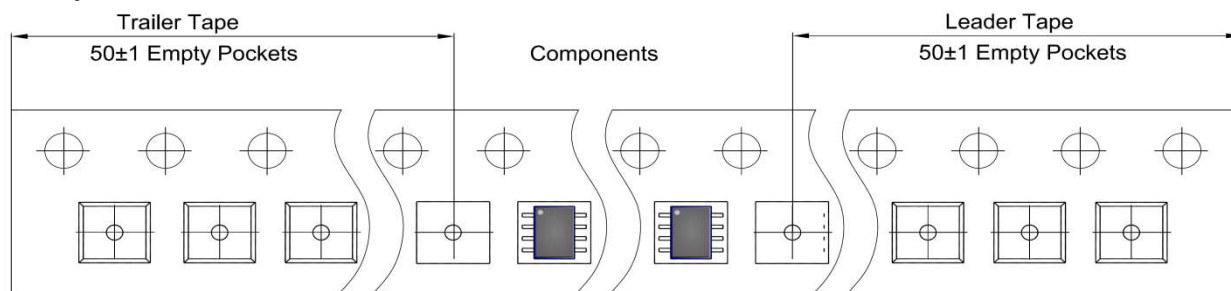
SOP-8 Tape and Reel

SOP-8 Embossed Carrier Tape

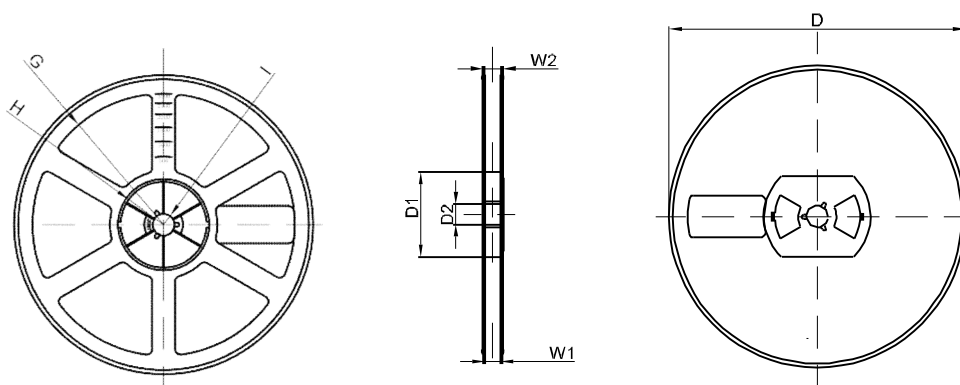


	DIMENSIONS ARE IN MILLIMETER									
TYPE	A	B	C	d	E	F	P0	P	P1	W
SOP-8	6.40	5.40	2.10	Ø1.50	1.75	5.50	4.00	8.00	2.00	12.00
TOLERANCE	±0.1	±0.1	±0.1	±0.1	±0.1	±0.1	±0.1	±0.1	±0.1	±0.1

SOP-8 Tape Leader and Trailer



SOP-8 Reel



	DIMENSIONS ARE IN MILLIMETER							
REEL OPTION	D	D1	D2	G	H	I	W1	W2
13" DIA	Ø330.00	100.00	13.00	R151.00	R56.00	R6.50	12.40	17.60
TOLERANCE	±2	±1	±1	±1	±1	±1	±1	±1